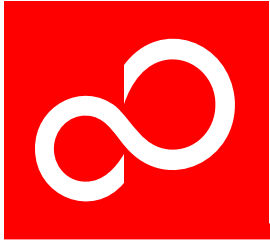


Fujitsu GDC Studio

Version 1.0.0.0





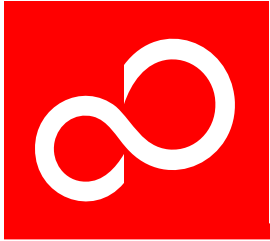
Fujitsu GDC Studio



Graphics Competence Center

■ Background Information :

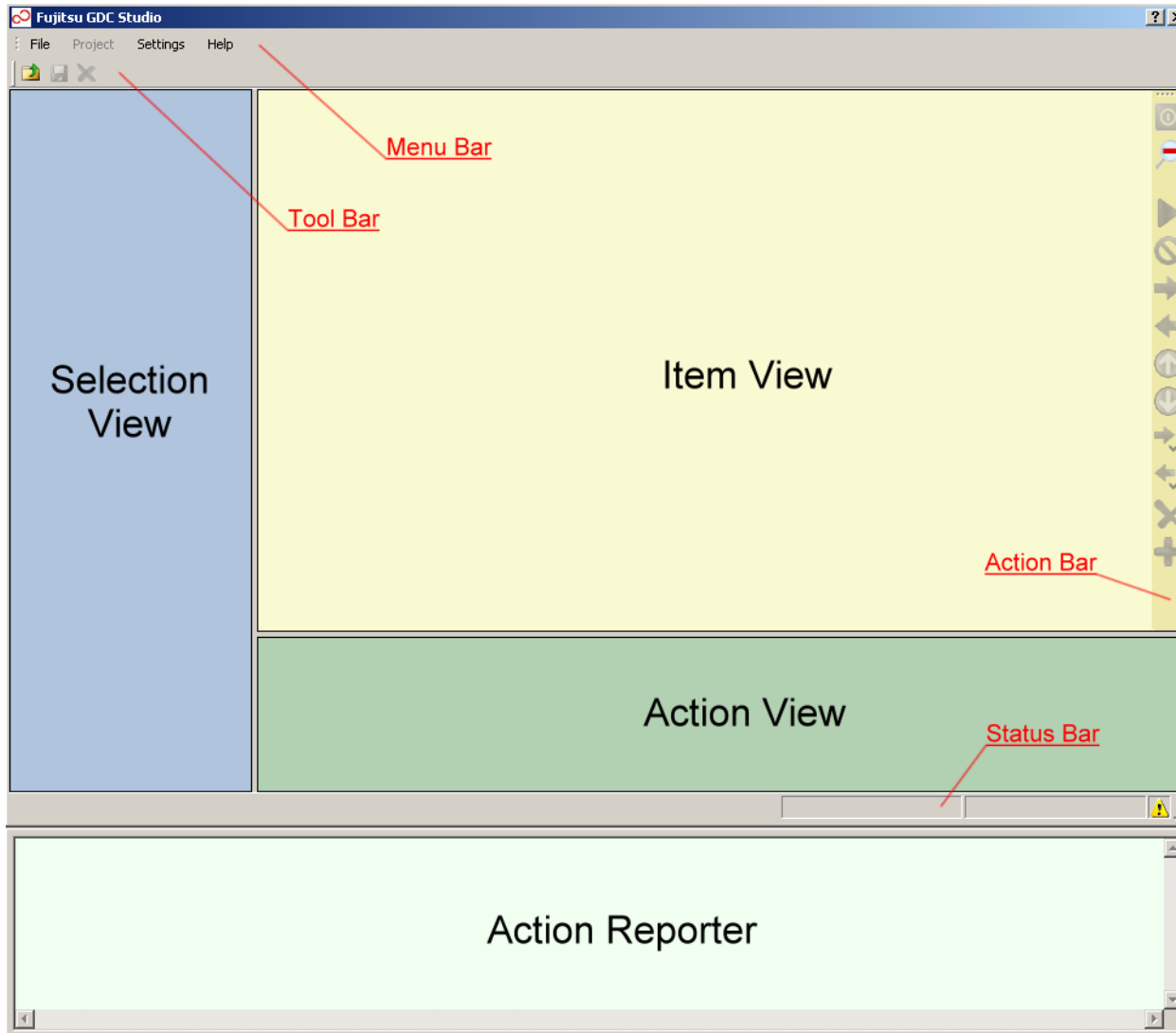
- The latest version (described here) is: Version 1.0.0.0
- Extensions to the current preview are in progress
- Changes and / or modifications may occur without prior notice

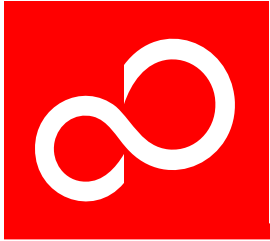


Fujitsu GDC Studio Layout



Graphics Competence Center





General Features (1)



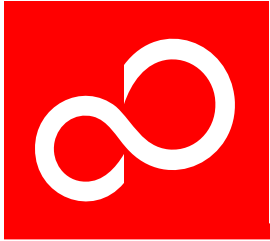
Graphics Competence Center

■ Flexible Project File Architecture

- Fujitsu GDC Studio's functionality is configured by loading a chip specific project file (.gdcproj)
- Project files are currently available for :
 - MB88F332 'Indigo',
 - MB86928 'Ruby'
- Additional project files for future Fujitsu chips are planned
- Project files can also be saved / reloaded when a specific chip status should be recorded

■ Available Features

- GUI based Register Debugger and Register Sequencer
- GUI based Image Manager and Font Manager
- GUI based memory inspection and editing functions:
 - Memory Editor and Hex Dump
 - Flash Editor, Flash Dump and Programmer



General Features (2)



Graphics Competence Center

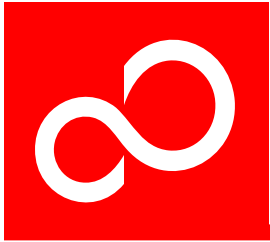
■ Modular Hardware Abstraction

- Depending on the chip design there are one or more of the following hardware access types possible :
 - SPI – Serial Peripheral Interface (connected via USB)
 - PCIe – Peripheral Component Interconnect Express
- Additional interface support is possible but currently not planned

■ Automatic Installation Setup Wizard available

■ User Manual with detailed Information available online

■ Release notes available online



Register Debugger - Layout



Graphics Competence Center

Fujitsu GDC Studio

File Project Settings Help

Register Debugger

- Stepper Motor Control
- A/D Converter
- Reload Timer Unit
- I2C Unit
- Sound Generator
- UART Unit
- Pulse Generator
- Chip Control
- Remote Handler
- Configuration FIFO
- Clock Modulator
- Clock Synthesis
- General Purpose IO
- Sprite Engine Ctrl
- Sprite Engine SAT
- Sprite Engine SS
- Timing Controller
- Signature Unit
- Color Lookup Table
- Dithering Unit
- Display Controller
- DMA Controller
- Memory Interface
- SPI Flash
- Run Length Decoder
- Command Sequencer
- Register Sequencer
 - panel_init_ET057003DM6_320x240
 - spe_reset_320x240
 - spe_test_color_bars_320x240
 - spe_test_single_color
 - spe_test_special_blink_32x240
 - spe_test_special_move_320x240
- Image Manager
- Font Manager
- Memory Editor
- Memory Dump

Name	Type	Bit Offset	Bit Width	Field Value	Register Value	Error
ADE7	RW	7	1	0		
ADE8	RW	8	1	0		
ADE9	RW	9	1	0		
ADE10	RW	10	1	0		
ADE11	RW	11	1	0		
ADCS0_ADCS1					0x00000000	
ACH_4_0	R	0	5	0		
S10	RW	5	1	0		
MD_1_0	RW	6	2	0		
RESERVED1	RSVD	8	1	0		
STRT	RW	9	1	0		
STS_1_0	RW	10	2	0		
PAUS	RW	12	1	0		
INTE	RW	13	1	0		
INT	RW	14	1	0		
BUSY	RW	15	1	0		
ADCR0_ADCR1						
D_7_0	R	0	8			
D_9_8	R	8	2			
ADCT0_ADCT1					0x0000102C	
ST_7_0	RW	0	8	44		
ST_9_8	RW	8	2	0		
CT_5_0	RW	10	6	4		
ADECH_ADSCH					0x00000000	
ANE_4_0	RW	0	5	0		
ANS_4_0	RW	8	5	0		

A/D channel setting register

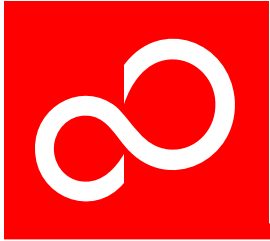
Bit Range 12 ... 8 Hexadecimal 7 Decimal 7 Discrete Values 0x0 0x1 0x2 0x3 0x4

Bit Width 5

Reset Value 0x0

Access Type RW 0 31

Indigo MB88F332

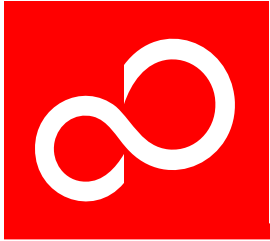


Register Debugger (1)



Graphics Competence Center

- **Covers the most essential hardware IP's of an available design**
 - e.g. MB88F332 'Indigo,, MB86928 'Ruby'
- **Detailed hardware information is visible for the selected ...**
 - IP / Component
 - Address Block
 - Register
 - Register Field
- **Practical register/field reads and writes**
 - Depending on the register properties, various 'simple to use' controls appear
 - The register access type is handled accordingly (R, RW, W, RSVD, ...)
- **Pop-up descriptions of the selected register fields are displayed**



Register Debugger (2)



Graphics Competence Center

■ Hardware access status supported

- An 'Error' column reporting the status of each access to the corresponding field is displayed on the far right
- An additional 'Action Reporting Window' can be opened if detailed access information is needed

■ Hardware connect / disconnect button available

- Enables a user to use Fujitsu GDC Studio with a different parallel target application
- Prevents hardware access problems if GDC Studio and a separate application use the same driver interface
- Fujitsu GDC Studio may be disconnected or reconnected at any time



Register Sequencer – Layout



Graphics Competence Center

Fujitsu GDC Studio

File Project Settings Help

Register Debugger

- Stepper Motor Control
- A/D Converter
- Reload Timer Unit
- I2C Unit
- Sound Generator
- UART Unit
- Pulse Generator
- Chip Control
- Remote Handler
- Configuration FIFO
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- Command Sequencer

Register Sequencer

- panel_init_ET057003DM6_320x240
- spe_reset_320x240
- spe_test_color_bars_320x240
- spe_test_single_color
- spe_test_special_blink_320x240
- spe_test_special_move_320x240

Image Manager

Font Manager

Memory Editor

Memory Dump

Register Name	Component Name	Address	Size	Register Value	Error
GeneralCtrl	Clock Synthesis	0x00014000	32 bit	0x00000002	
NominalFrequency	Clock Synthesis	0x00014004	32 bit	0x00130200	
HTP	Display Controller	0x00034004	32 bit	0x01980000	
HDP	Display Controller	0x00034008	32 bit	0x00000140	
HSP_HSW_VSW	Display Controller	0x0003400C	32 bit	0x03280161	
VTR	Display Controller	0x00034010	32 bit	0x01040000	
VDP_VSP	Display Controller	0x00034014	32 bit	0x00F000F4	
DCM0	Display Controller	0x00034000	32 bit	0x80060004	
DLS	Display Controller	0x00034210	32 bit	0x00000001	
LAETC	Display Controller	0x00034240	32 bit	0x80000000	
PFD	Display Controller	0x00034364	32 bit	0x00000000	
Interrupt_Enable	Display Controller	0x00034204	32 bit	0x00000100	
SPEDPAR	Sprite Engine Ctrl	0x00020024	32 bit	0x00000140	
DIR_RBM_CTRL	Timing Controller	0x0002852C	32 bit	0x00000009	
DIR_PIN0_CTRL	Timing Controller	0x00028534	32 bit	0x00000090	
DIR_PIN1_CTRL	Timing Controller	0x00028538	32 bit	0x00000090	
DIR_PIN2_CTRL	Timing Controller	0x0002853C	32 bit	0x00000090	
DIR_PIN3_CTRL	Timing Controller	0x00028540	32 bit	0x00000090	
DIR_PIN4_CTRL	Timing Controller	0x00028544	32 bit	0x00000090	
DIR_PIN5_CTRL	Timing Controller	0x00028548	32 bit	0x00000090	
DIR_PIN6_CTRL	Timing Controller	0x0002854C	32 bit	0x00000090	
DIR_PIN7_CTRL	Timing Controller	0x00028550	32 bit	0x00000090	
DIR_PIN8_CTRL	Timing Controller	0x00028554	32 bit	0x00000090	
DIR_PIN9_CTRL	Timing Controller	0x00028558	32 bit	0x00000091	
DIR_PIN10_CTRL	Timing Controller	0x0002855C	32 bit	0x00000090	
DIR_PIN11_CTRL	Timing Controller	0x00028560	32 bit	0x00000090	
DIR_PIN12_CTRL	Timing Controller	0x00028564	32 bit	0x00100091	

Chip Id: MB88F332

Codename: Indigo

Version: 0.1

Sequence Execution Mode: Default, Independent

Delay

Save Sequence Close Sequence Activate Sequence Rename Sequence

Indigo MB88F332



Register Sequencer - Debug



Graphics Competence Center

Fujitsu GDC Studio

File Project Settings Help

Register Debugger

- Stepper Motor Control
- A/D Converter
- Reload Timer Unit
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- Pulse Generator
- Chip Control
- Remote Handler
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- Clock Modulator
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- General Purpose IO
- Sprite Engine Ctrl
- Sprite Engine SAT
- Sprite Engine SS
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- Color Lookup Table
- Dithering Unit
- Display Controller
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- Memory Interface
- SPI Flash
- Run Length Decoder
- Command Sequencer

Register Sequencer

- panel_init_ET057003DM6_320x240
- spe_reset_320x240
- spe_test_color_bars_320x240
- spe_test_single_color
- spe_test_special_blink_32x240
- spe_test_special_move_320x240
- Example Sequence

Image Manager

- Font Manager
- Memory Editor
- Memory Dump

Register Name	Component Name	Address	Size	Register Value	Error
ChipInfo	Chip Control	0x00010000	32 bit	0x20080000	
FIFOthresh	Remote Handler	0x0001100C	32 bit	0x00000F0F	
SPELUTS	Sprite Engine Ctrl	0x00026000	32 bit	0xFF000000	
SPELUTS	Sprite Engine Ctrl	0x00026004	32 bit	0x0000FF00	
SPELUTS	Sprite Engine Ctrl	0x00026008	32 bit	0x00FF0000	
SPESCR2	Sprite Engine SAT	0x00022008	32 bit	0x00000000	
InterruptStatusW0	Signature Unit	0x0002A05C	32 bit	0x000001FF	
ColourIndexElement	Color Lookup Table	0x0002C000	32 bit	0x00000000	
ColourIndexElement	Color Lookup Table	0x0002C004	32 bit	0x00000000	
ColourIndexElement	Color Lookup Table	0x0002C008	32 bit	0x00000000	
ColourIndexElement	Color Lookup Table	0x0002C00C	32 bit	0x00000000	
Dither Control	Dithering Unit	0x0002E000	32 bit	0x00000001	
Software Delay Element	-	-	-	100	
HDP	Display Controller	0x00034004	32 bit	0x031F0000	
HDP	Display Controller	0x00034008	32 bit	0x0000027F	
HSP_HSW_VSW	Display Controller	0x0003400C	32 bit	0x015F028F	
VTR	Display Controller	0x00034010	32 bit	0x020C0000	
VDP_VSP	Display Controller	0x00034014	32 bit	0x01DF01E9	
Software Delay Element	-	-	-	200	
Status	Display Controller	0x00034200	32 bit	0x00000000	

Sequence Execution Mode

Default, Independent

Delay

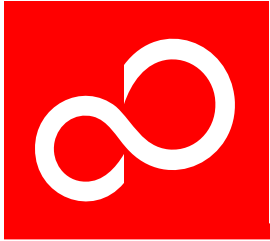
Chip Id MB88F332

Codename Indigo

Version 0.1

Save Sequence Close Sequence Activate Sequence Rename Sequence

Indigo MB88F332



Register Sequencer (1)



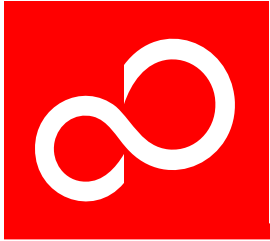
Graphics Competence Center

■ Easy creation of register sequences

- Allows a user to define and create new register sequences
- Any of the available register sequences can be selected to get input focus
- The Register Debugger is used to select and add the required registers to the currently active sequence
- If a special non-listed address (e.g. memory) should be accessed a user defined sequence element can be inserted allowing to configure access type, size, mode, ...

■ Register sequence management implemented

- Register sequences can be loaded and saved independently
- Sequence names can be created and modified
- Individual sequence items can be repositioned or removed
- Sequence items can also be deactivated to prevent from execution
- Values, Masks, Loop counter, ... of the sequence items can be manipulated



Register Sequencer (2)



Graphics Competence Center

■ Execution of selected register sequences

- Play and Stop buttons available when connection to the target chip is detected
- Special modes and functions are available, depending on the supported chip



Register Sequencer (3)



Graphics Competence Center

■ Sequence debugging

- It is also possible to debug register sequences
- For this the following debugging functionality is available :
 - Breakpoints
 - 'Single Step'
 - 'Execute to next Breakpoint'
 - 'Stop Sequence'
- Furthermore special sequence items are implemented which support debugging :
 - 'Write' register element
 - 'Read' register element
 - 'Polling Register' elements with a user defined mask and counter
 - 'Write Repeat' element
 - 'Write Repeat Increment' with an address autoincrement

All Elements above are also available User Defined with a definable address and register size

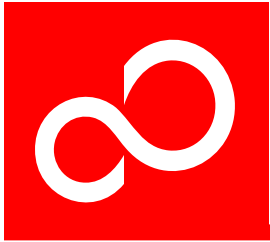
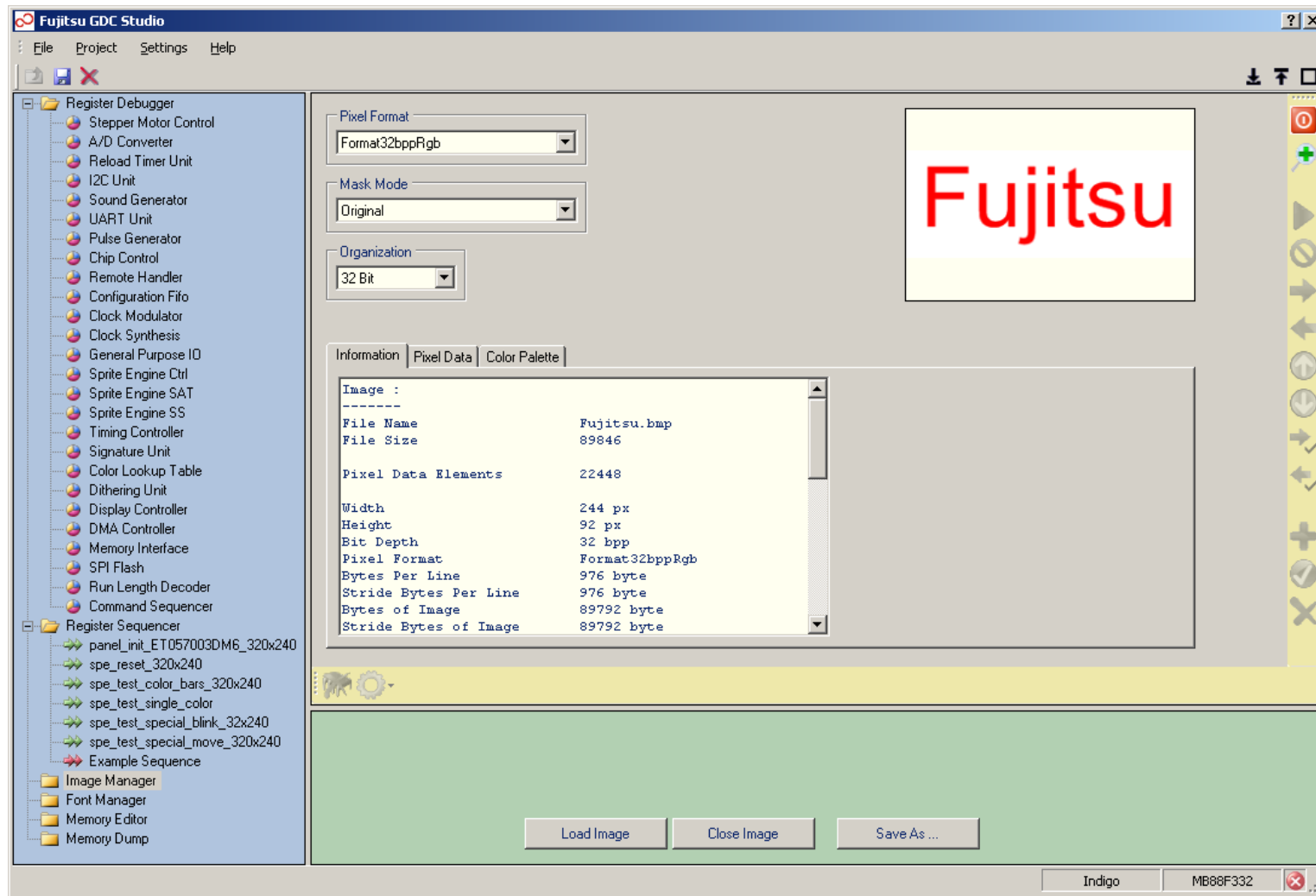


Image Manager - Layout



Graphics Competence Center





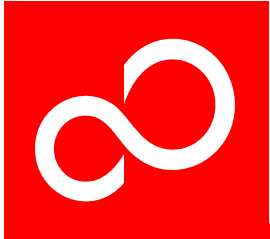
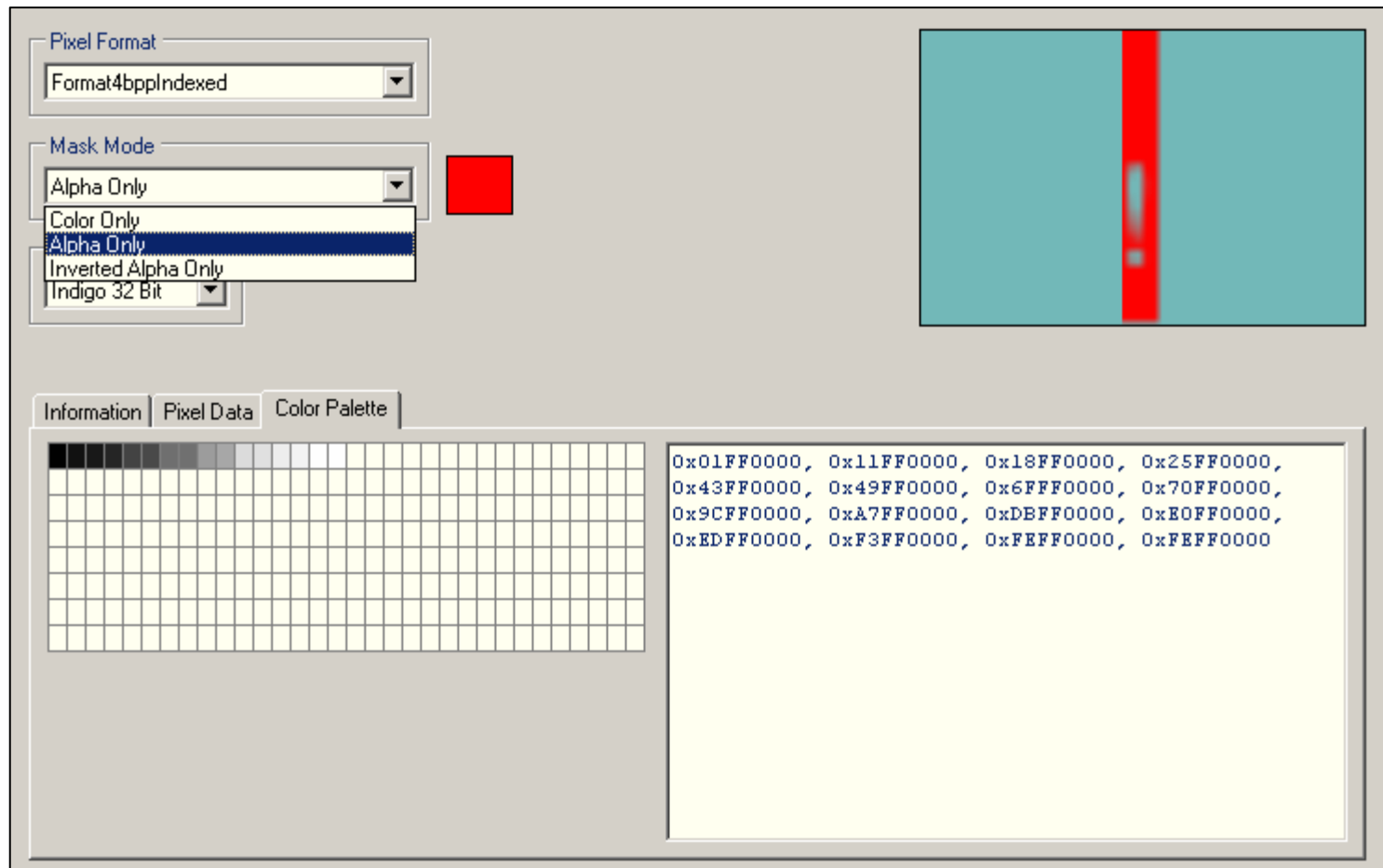


Image Manager – Pages (2)



Graphics Competence Center



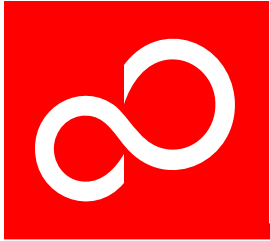


Image Manager (1)



Graphics Competence Center

■ Extract image information for application development

- Several pages (tabs) provide functions to extract information from an image file and to make this available for a target application
- Automatic source ('C') code generation of image information is possible
- 32 bit organized images can also be saved as binary file (.gdc32dat)
- An 'Information Page' is available to obtain general image information
- A 'Pixel Data Page' is available to extract the core pixel values in a specific organization (8, 16, 24 or 32 bit array)
- A 'Color Palette Page' is available to visualize the colors of indexed format pictures and to create the corresponding Color-Lookup-Tables (CLUTs)

■ Conversion of pixel data into a chip-specific structure

- Some chips (e.g. Indigo) require a special pixel data arrangement in memory which can be created/converted by this tool

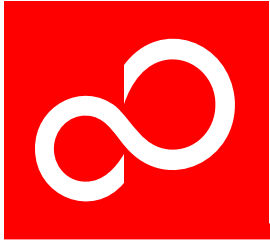


Image Manager (2)



Graphics Competence Center

■ Conversion into different pixel formats

- Images can be read from different image/file formats
- Images can be converted between different pixel formats

■ Depending on the input image and the pixel format different 'Mask Modes' will be supported

- Original
- Color Only
- Alpha Only
- Inverted Alpha Only
- Alpha + Color

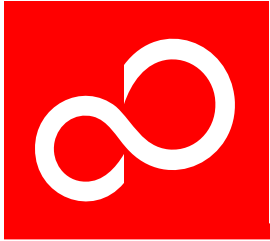


Image Manager (3)



Graphics Competence Center

■ Support for images of the following file types:

- Bmp Bitmap
- Png Portable Network Graphics
- Tiff Tagged Image File Format
- Jpeg Joint Photographic Expert Group
- Gif Graphics Interchange Format

■ Support for the following pixel formats:

- 1 bpp (bit-per-pixel), indexed
- 4 bpp, indexed
- 8 bpp, indexed
- 16 bpp, different formats
- 24 bpp, RGB
- 32 bpp, ARGB

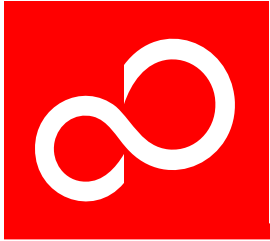


Image Manager (4)

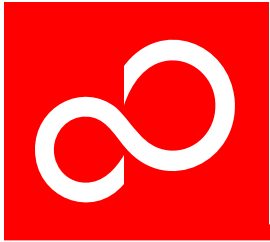


Graphics Competence Center

■ Support for the following output pixel organization:

- 8 Bit
- 16 Bit
- 32 Bit
- Indigo 32 Bit (Indigo Only)
- Indigo 32 Bit RLD (Indigo Only)
- Ruby 32 Bit ARGB (Ruby Only)
- Ruby 32 Bit ABGR (Ruby Only)
- Ruby 32 Bit RGBA (Ruby Only)

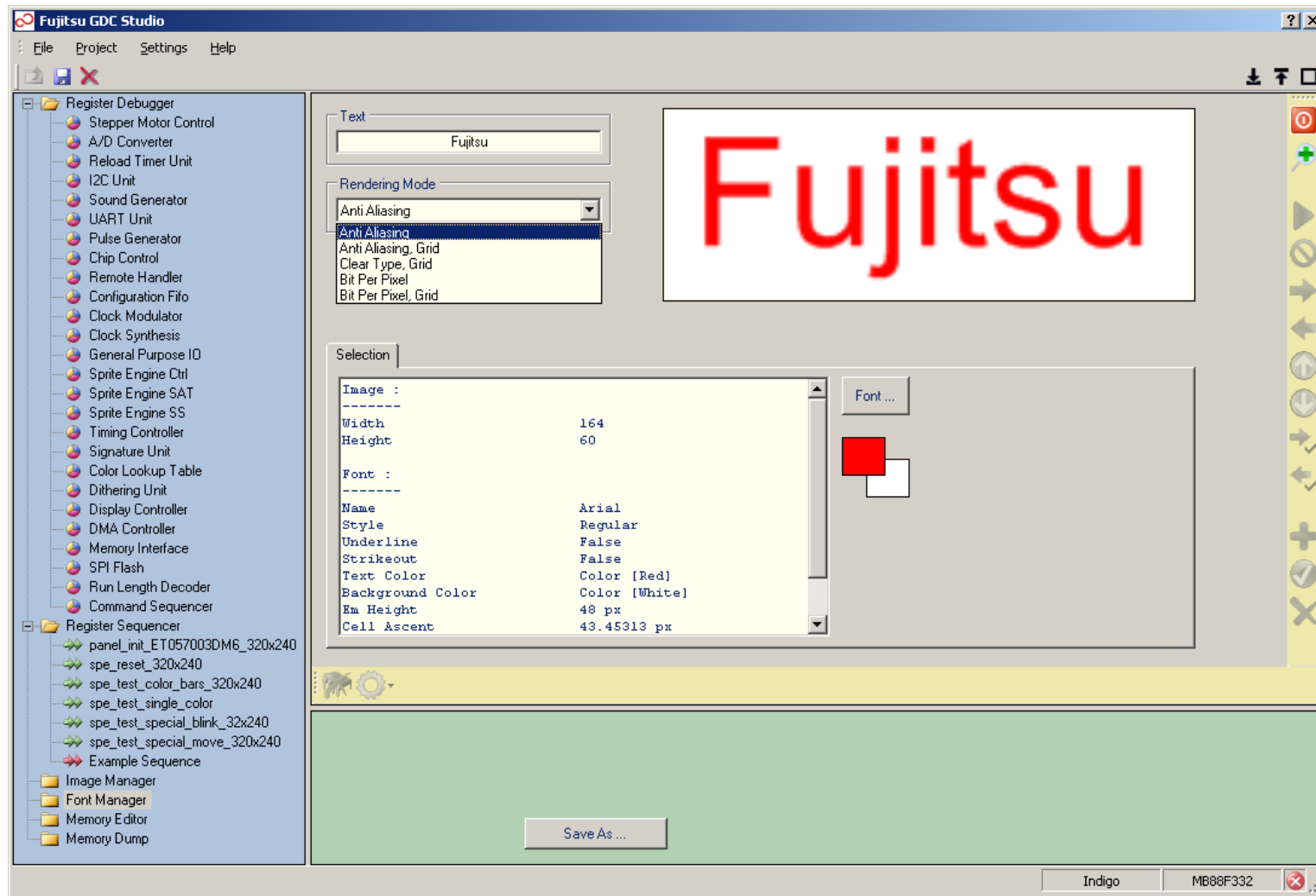
■ Any changes are updated immediately in the Picture Box and the corresponding tab pages

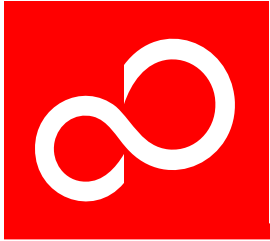


Font Manager - Layout



Graphics Competence Center





Font Manager (1)

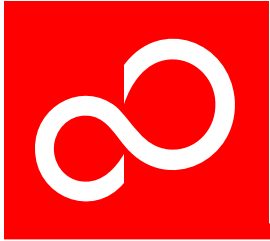


Graphics Competence Center

■ Support for sprite generation during application development

- The Font Manager is used to simply generate attractive letters, numbers or more complex texts
- The following steps are suggested:
 1. Select a system font (and a specific character size)
(if a special font is needed, copy it to the system font directory first!)
 2. Select the required text color
 3. Choose the destination image background color
 4. Select the required rendering mode
 5. Save the resulting output image into a 32 bit (ARGB) file
 6. Load the stored file into the Image Converter for further processing

■ All changes made are updated immediately in the Picture Box



Font Manager (2)



Graphics Competence Center

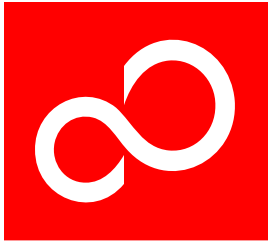
■ The following rendering modes are supported:

- Anti-aliasing
- Anti-aliasing (Grid)
- Clear Type (Grid)
- Bit Per Pixel
- Bit Per Pixel (Grid)

■ The output image can be saved in one of the following file formats:

- Bmp Bitmap
- Png Portable Network Graphics
- Tiff Tagged Image File Format
- Jpeg Joint Photographic Expert Group
- Gif Graphics Interchange Format





Flash Editor - Layout



Graphics Competence Center

Fujitsu GDC Studio

File Project Settings Help

Register Debugger

- Stepper Motor Control
- A/D Converter
- Reload Timer Unit
- I2C Unit
- Sound Generator
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- Pulse Generator
- Chip Control
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- Configuration File
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- SPI Flash
- Run Length Decoder
- Command Sequencer

Register Sequencer

- panel_init_ET057003DM6_320x240
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- spe_test_single_color
- spe_test_special_blink_32x240
- spe_test_special_move_320x240
- Example Sequence

Image Manager

Font Manager

Flash Editor

Flash Dump

	0	1	2	3	4	5	6	7
0x000A0000	12345678	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0020	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0040	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0060	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0080	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A00A0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A00C0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A00E0	FFFFFFFF	FFFFFFFF	FFFFFFFF	87654321	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0100	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0120	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0140	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0160	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0180	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A01A0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A01C0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A01E0	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0200	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0220	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0240	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
0x000A0260	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF

Erase Flash Chip

Erase Single Flash Sector

None

None

0

1

2

3

4

5

Offset (Hex)

0

Value (Hex)

87654321

Read Memory Block

Flash Memory Block

Indigo MB88F332

Scanning Flash Memory Block for Content Detected

Scanning Memory Block and Flash Memory Block for Difference Detected

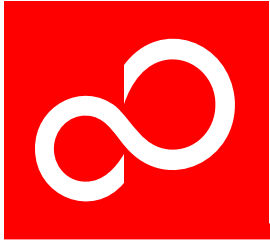
Start saving corresponding Sector Data Done

Modifying saved Data Done

Erasing corresponding Sectors Done

Flashing modified Data to Flash Memory Done

PROCESSING FINISHED with SUCCESS



Memory / Flash Editor



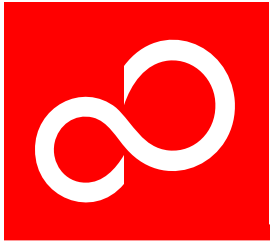
Graphics Competence Center

■ Useful for several tasks

- Supports debugging and validation for both hardware and software, e.g. by dumping the memory content to check the proper loading of sprites
- Manipulation of data stored in either RAM or flash memory by:
 - reading/writing single memory cells (4 bytes each) or
 - reading/writing complete memory blocks from/to a specified address
 - Limited to 512 items per block

■ Using the editor is straightforward:

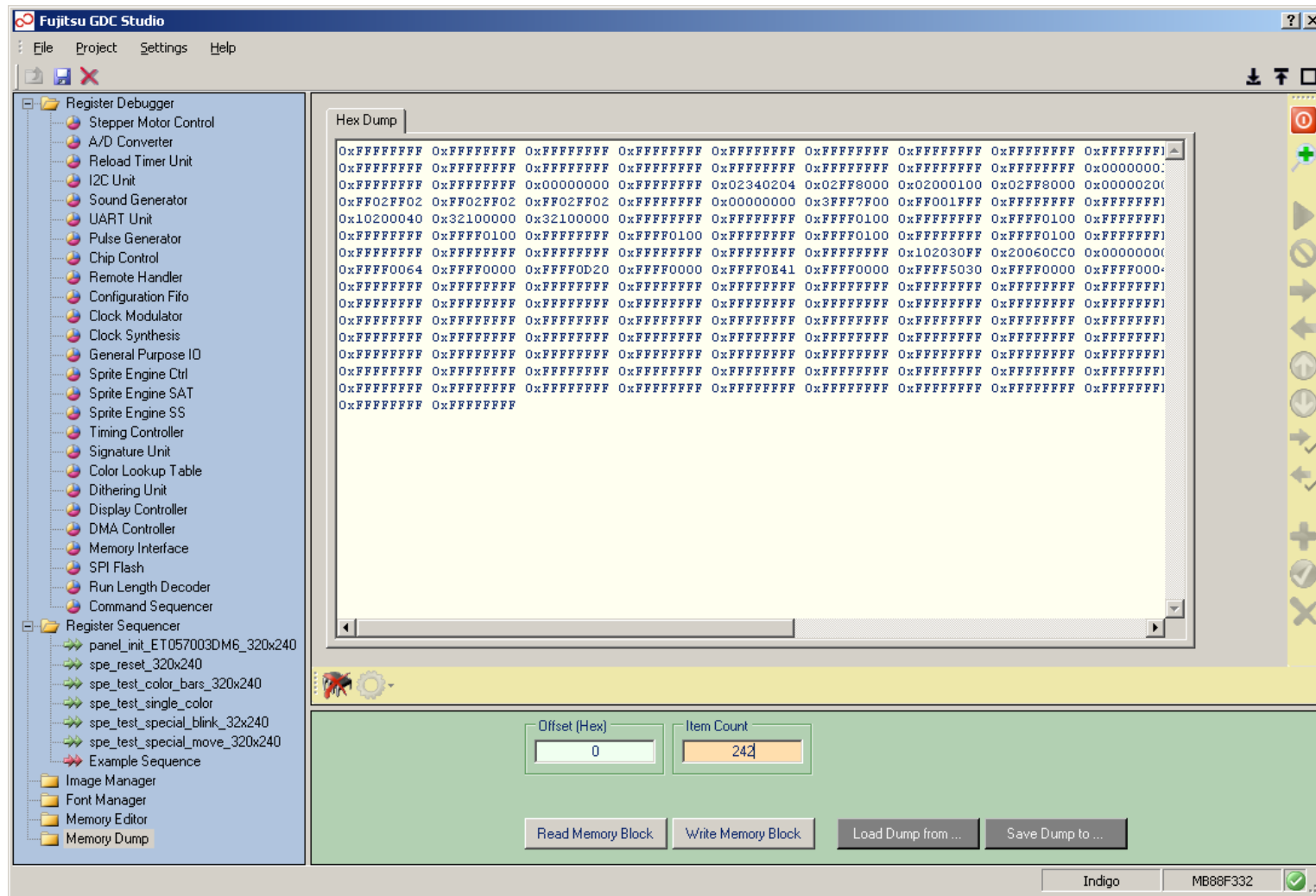
- Enter the start address (of register, RAM or flash memory)
- Insert the required number of items to be read
(an item is the smallest unit to be dumped = 4 bytes width)
- Read out the memory block into virtual memory by pressing the corresponding button
- Manipulate single items
- Write the manipulated virtual memory block (or parts of it) back to the start address or any other specified address



Memory Dump - Layout



Graphics Competence Center

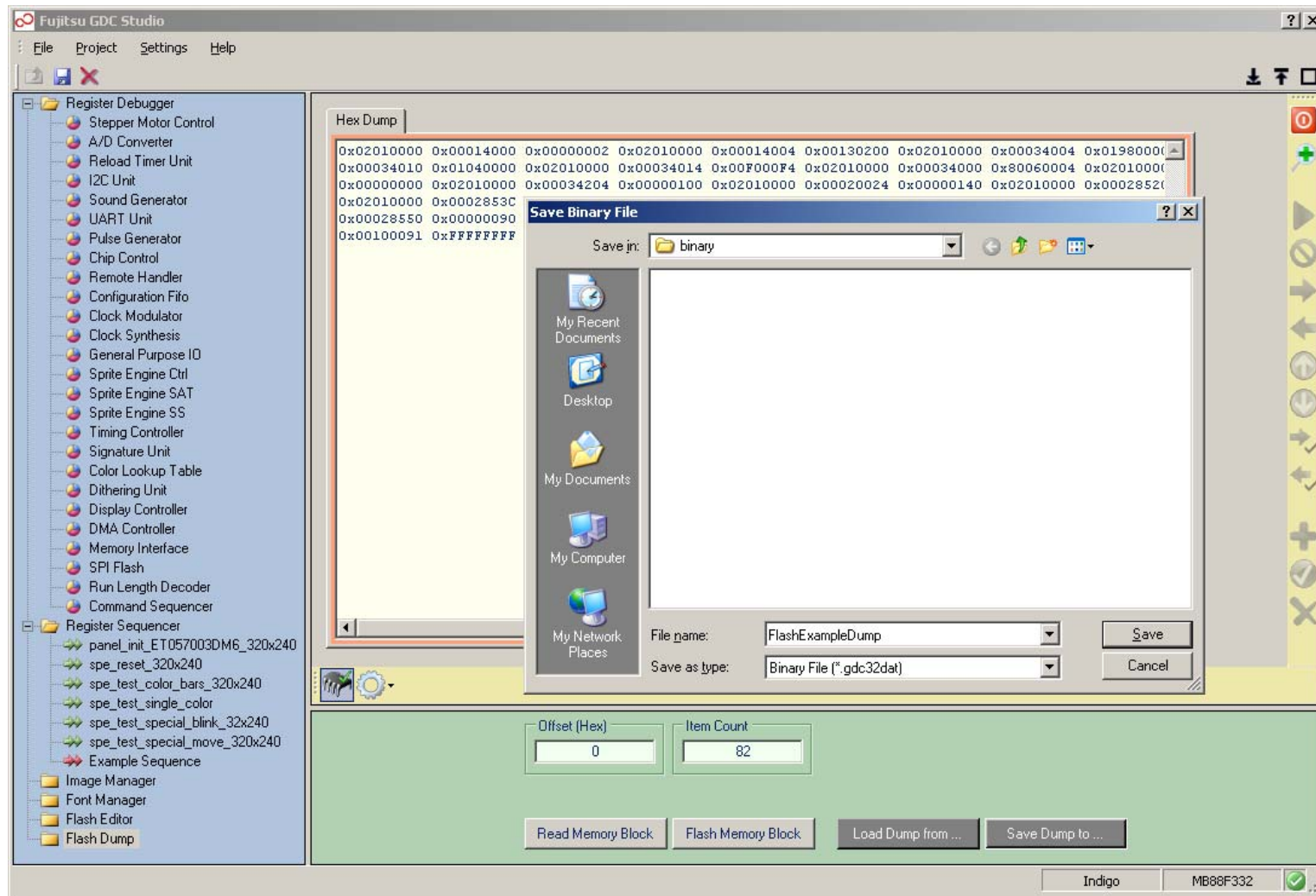


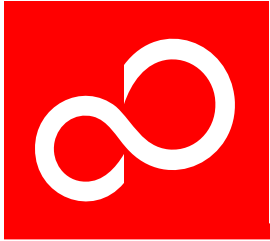


Flash Dump - Layout



Graphics Competence Center





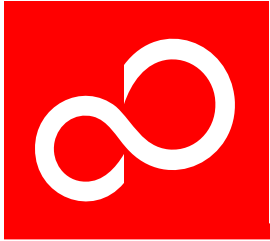
Memory / Flash Dump



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■ Supported Features :

- Provides an overview of large memory blocks, i.e. many more items can be dumped and listed on the screen than in the Memory Editor (currently limited to 8MByte)
- Reads register, memory or flash areas
- Saves the dumped data into binary files (.gdc32dat)
- Reloads binary files into the dump view – also converted images
- Loads Register Sequencer files (interpreted as command list values on Indigo)
- Writes the dump view content to a specified address in the register, memory or flash area
- An internal state machine is implemented to optimize data writing into flash memory (e.g. check if empty, check for new content before writing, automatic merges of new data and already existing identical data based on a read and comparison of corresponding sectors, ...)



Tool Environment (1)



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■ GDC Studio runs on Microsoft operating systems

- Windows 2000
- Windows XP
- Windows Vista (when supported from the interface driver)
- GDC Studio's Setup Wizard provides an automatic installation process

■ Interface between a PC/Laptop and the MB88F332 (Indigo):

SPI

- USB to SPI converter box 'Aardvark I2S/SPI Host Adapter'
- GDC Studio uses the USB driver provided with the 'Aardvark' hardware
- Must be purchased directly from the company 'TOTAL PHASE'
- http://www.totalphase.com/products/aardvark_i2cspi/
- Hardware is not delivered with the tool and is not included in the license fee



Tool Environment (2)



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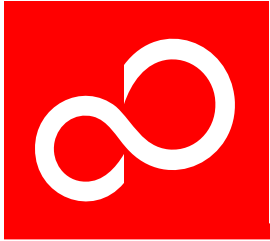
■ Interface between a PC/Laptop and the MB86298 (Ruby):

SPI

- USB to SPI converter box 'Aardvark I2S/SPI Host Adapter'
- GDC Studio uses the USB driver provided with the 'Aardvark' hardware
- Must be purchased directly from the company 'TOTAL PHASE'
- http://www.totalphase.com/products/aardvark_i2cspi/
- Hardware is not delivered with the tool and is not included in the license fee

PCIe

- For this chip design the Fujitsu GD Studio supports the PCIe connection of the Ruby Evaluation Board directly



Licensing Model



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- An installation must be licensed for every PC workplace (machine)
- Licenses for multiple workplaces (groups) are also possible
- A free tool is provided which supports the authorization procedure that extracts the required information from the PC workplace hardware:
 - 'Fujitsu GDC Studio Authorization Support Tool'
- This information can be selected and sent to Fujitsu GCC to get an authorization for the use of Fujitsu GDC Studio
- The license fee depends on # installations/PC workplaces:
 - Licenses are available for groups of:
 - up to 4 workplaces
 - up to 6 workplaces
 - up to 8 workplaces
 - up to 10 workplaces
 - up to 12 workplaces
 - up to 14 workplaces
 - up to 16 workplaces



THE POSSIBILITIES ARE INFINITE